CLAIMS

1. A data transmission/reception system for transferring a clock signal and a plurality of data signals which are in synchronization with the clock signal, comprising:

a clock reception system for receiving the clock signal;

a plurality of data reception systems for receiving corresponding data signals among the plurality of data signals;

a clock transmission system for transmitting the clock signal supplied from the clock reception system to a clock signal transfer path at a small amplitude; and

a plurality of data transmission systems for transmitting the data signals supplied from corresponding data reception systems among the plurality of data reception systems to a data signal transfer path at a small amplitude,

wherein the clock transmission system and the plurality of data transmission systems are respectively connected to a first power supply and a second power supply for operations,

the clock transmission system includes

a clock driver circuit for driving the clock signal transfer path according to the clock signal supplied from the clock reception system, and

a feedback circuit for determining a high level voltage and a low level voltage of the clock signal transfer path to generate at least one control signal which is to be supplied to the clock driver circuit such that a high level voltage of the clock signal which is transmitted to the clock signal transfer path is equal to a first reference voltage which is lower than a voltage of the first power supply, and a low level voltage of the clock signal which is transmitted to the clock signal transfer path is equal to a second reference voltage which is higher than a voltage of the second power supply, and

each data transmission system includes a data driver circuit for driving the data

signal transfer path according to a data signal supplied from a corresponding data reception system among the plurality of data reception systems while amplitude control is performed on the data signal which is to be transmitted to the data signal transfer path based on a control signal generated by the feedback circuit.

2. The data transmission/reception system of claim 1, wherein:

the clock driver circuit includes

a first switch interposed between the first power supply and the clock signal transfer path,

a second switch interposed between the clock signal transfer path and the second power supply,

a first driving pulse generation circuit for driving the first switch,

a second driving pulse generation circuit for driving the second switch,

a third switch which is turned on when a high level voltage is output to the clock signal transfer path and which is turned off when a low level voltage is output to the clock signal transfer path,

a fourth switch which is turned off when a high level voltage is output to the clock signal transfer path and which is turned on when a low level voltage is output to the clock signal transfer path,

a first buffer for supplying the first reference voltage to the clock signal transfer path through the third switch, and

a second buffer for supplying the second reference voltage to the clock signal transfer path through the fourth switch,

the feedback circuit includes

a detection circuit for detecting the high level voltage and the low level voltage of the clock signal transfer path, and

first and second amplifiers for amplifying differences between a high level voltage and a low level voltage detected by the detection circuit and the first and second reference voltages, respectively, to output the amplified differences as first and second control signals,

the first driving pulse generation circuit controls the width of a pulse which drives the first switch based on the first control signal such that the high level voltage of the clock signal transfer path is equal to the first reference voltage, and

the second driving pulse generation circuit controls the width of a pulse which drives the second switch based on the second control signal such that the low level voltage of the clock signal transfer path is equal to the second reference voltage.

3. The data transmission/reception system of claim 2, wherein:

each of the data driver circuits includes

a fifth switch interposed between the first power supply and the data signal transfer path,

a sixth switch interposed between the data signal transfer path and the second power supply,

a third driving pulse generation circuit for driving the fifth switch,

a fourth driving pulse generation circuit for driving the sixth switch,

a seventh switch which is turned on when a high level voltage is output to the data signal transfer path and which is turned off when a low level voltage is output to the data signal transfer path,

an eighth switch which is turned off when a high level voltage is output to the data signal transfer path and which is turned on when a low level voltage is output to the data signal transfer path,

a third buffer for supplying the first reference voltage to the data signal

transfer path through the seventh switch, and

a fourth buffer for supplying the second reference voltage to the data signal transfer path through the eighth switch,

the third driving pulse generation circuit controls the width of a pulse which drives the fifth switch based on the first control signal such that the high level voltage of the data signal transfer path is equal to the first reference voltage, and

the fourth driving pulse generation circuit controls the width of a pulse which drives the sixth switch based on the second control signal such that the low level voltage of the data signal transfer path is equal to the second reference voltage.

4. The data transmission/reception system of claim 1, wherein:

the clock driver circuit includes

a first switch interposed between the first power supply and the clock signal transfer path,

a second switch interposed between the clock signal transfer path and the second power supply,

a first driving pulse generation circuit for driving the first switch and the second switch,

a third switch which is turned on when a high level voltage is output to the clock signal transfer path and which is turned off when a low level voltage is output to the clock signal transfer path,

a fourth switch which is turned off when a high level voltage is output to the clock signal transfer path and which is turned on when a low level voltage is output to the clock signal transfer path,

a first buffer for supplying the first reference voltage to the clock signal transfer path through the third switch, and

a second buffer for supplying the second reference voltage to the clock signal transfer path through the fourth switch,

the feedback circuit includes

a circuit for detecting the amplitude of a clock signal on the clock signal transfer path, and

a first amplifier for amplifying the difference between the detected amplitude and a desired output amplitude to output the amplified difference as a first control signal, and

the first driving pulse generation circuit controls the width of a pulse which drives the first and second switches based on the first control signal such that the amplitude of the clock signal on the clock signal transfer path is equal to the desired output amplitude.

5. The data transmission/reception system of claim 4, wherein:

each of the data driver circuits includes

a fifth switch interposed between the first power supply and the data signal transfer path,

a sixth switch interposed between the data signal transfer path and the second power supply,

a second driving pulse generation circuit for driving the fifth switch and the sixth switch,

a seventh switch which is turned on when a high level voltage is output to the data signal transfer path and which is turned off when a low level voltage is output to the data signal transfer path,

an eighth switch which is turned off when the high level voltage is output to the data signal transfer path and which is turned on when the low level voltage is output to the data signal transfer path,

a third buffer for supplying the first reference voltage to the data signal transfer path through the seventh switch, and

a fourth buffer for supplying the second reference voltage to the data signal transfer path through the eighth switch, and

the second driving pulse generation circuit controls the width of a pulse which drives the fifth switch and the sixth switch based on the first control signal such that the amplitude of the data signal on the data signal transfer path is equal to the desired output amplitude.

6. The data transmission/reception system of claim 4, wherein:

the feedback circuit further includes a second amplifier for amplifying the difference between a low level voltage of the clock signal transfer path and the second reference voltage to output the amplified difference as a second control signal;

the clock driver circuit further includes a first voltage-controlled current source interposed between the second switch and the second power supply; and

the driving capacity of the first voltage-controlled current source is controlled based on the second control signal such that the low level voltage of the clock signal transfer path is equal to the second reference voltage.

7. The data transmission/reception system of claim 6, wherein:

each of the data driver circuits includes

a fifth switch interposed between the first power supply and the data signal transfer path,

a sixth switch and a second voltage-controlled current source which are interposed in series between the data signal transfer path and the second power supply,

a second driving pulse generation circuit for driving the fifth switch and

the sixth switch,

a seventh switch which is turned on when a high level voltage is output to the data signal transfer path and which is turned off when a low level voltage is output to the data signal transfer path,

an eighth switch which is turned off when a high level voltage is output to the data signal transfer path and which is turned on when a low level voltage is output to the data signal transfer path,

a third buffer for supplying the first reference voltage to the data signal transfer path through the seventh switch, and

a fourth buffer for supplying the second reference voltage to the data signal transfer path through the eighth switch,

the second driving pulse generation circuit controls the width of a pulse which drives the fifth switch and the sixth switch based on the first control signal such that the amplitude of the data signal on the data signal transfer path is equal to the desired output amplitude; and

the driving capacity of the second voltage-controlled current source is controlled based on the second control signal such that the low level voltage of the data signal transfer path is equal to the second reference voltage.

8. The data transmission/reception system of claim 4, wherein:

the clock reception system includes a delay circuit for delaying the received clock signal by a time period determined according to the first control signal generated by the feedback circuit; and

each of the plurality of data reception systems includes a latch for sampling the received data signal in synchronization with a delayed clock signal output from the delay circuit.